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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,224	02/14/2002	Katsuya Sakayori	DAIN : 666	6194

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,224	SAKAYORI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-104* is/are pending in the application.

4a) Of the above claim(s) *1-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *57-104* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group II (claims 57-104) in the reply filed on February 14, 2002 is acknowledged. The traversal is on the ground(s) that the search and examination of the entire application could be made without serious burden. This is not found persuasive because they have acquired a separate status in the art as shown by their classification.

2. The requirement is still deemed proper and is therefore made FINAL.

Information Disclosure Statement

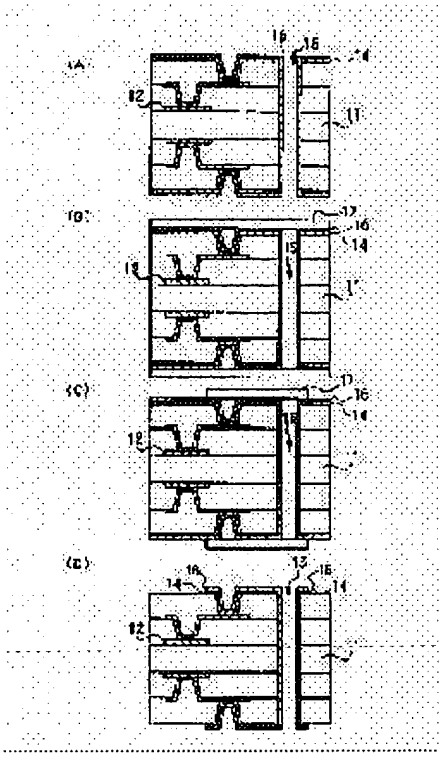
3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 77, 78, 79, 80, 81 and 82 are rejected under 35 U.S.C. 102(b) as being anticipated by Takashi et al., Patent Abstract of Japan Publication number: 2000-183523.



6. Takashi discloses a semiconductor process as claimed. See **Drawing 1(a)-1(e)**.

Pertaining to claim 57, Takashi teaches a process for producing an electronic component, comprising the steps of:

wet etching (see [0019]) a laminate of conductive inorganic material layer **12** insulating layer **11** conductive inorganic material layer or a laminate of conductive inorganic material layer insulating layer to pattern the conductive inorganic material layer; and

then performing wet etching to pattern the insulating layer, wherein

the insulating layer in the laminate is wet etchable and has a single-layer structure or a laminate structure of two or more insulation unit layers, and

the patterning of the insulating layer by the wet etching is carried out using a dry film resist **17**.

7. Pertaining to claim 58, Takashi teaches the process for producing an electronic component according to claim 57, wherein the surface of the dry film resist has fine concaves and convexes (the Examiner takes the position that all materials reveal fine concaves and convexes at a relative scale, because Applicants do not disclose a scale the claim is rejected as discussed, also see [0022]).

8. Pertaining to claim 59, Takashi teaches the process for producing an electronic component according to claim 58, wherein the fine concaves and convexes are provided by embossing (please note that embossing is merely nothing more that applying pressure).

9. Pertaining to claim 60, Takashi teaches the process for producing an electronic component according to claim 57, wherein the dry film resist is developable with an aqueous solution and can be separated by the aqueous solution.

10. Pertaining to claim 61, Takashi teaches the process for producing an electronic component according to claim 60, wherein the aqueous solution is an aqueous basic solution.

11. Pertaining to claim 62, Takashi teaches the process for producing an electronic component according to claim 57, wherein the insulating layer is patterned by the wet etching in such a manner that a dry film resist is laminated under reduced pressure onto the laminate in

which the conductive inorganic material layer has been patterned, followed by wet etching of the laminate of the dry film resist.

12. Pertaining to claim 63, Takashi teaches the process for producing an electronic component according to claim 61, wherein the laminate of the dry film resist is wet etched by a method wherein, after the laminate of the dry film resist is exposed and developed to perform patterning, in order to improve the resistance of the dry film resist to the etchant for the insulating layer, treatment selected from ultraviolet light irradiation, heat treatment, and a combination of ultraviolet light irradiation with heat treatment is carried out ([0030], i.e., a mercury lamp emits ultraviolet light radiation) .

13. Pertaining to claim 64, Takashi teaches the process for producing an electronic component according to claim 57, wherein the insulating layer in the laminate as the starting material has a thickness of 3 to 500 μm (Example 1).

14. Pertaining to claim 65, Takashi teaches the process for producing an electronic component according to claim 57, wherein the thickness of the dry film resist is 1.1 to 5 times that of one conductive inorganic material layer in the laminate as the starting material.

15. Pertaining to claim 66, Takashi teaches the process for producing an electronic component according to claim 57, wherein the time necessary for wet etching of the insulating layer is not less than 10 sec and not more than 30 min.

16. Pertaining to claim 67, Takashi teaches the process for producing an electronic component according to claim 57, wherein the temperature in the wet etching of the insulating layer is not less than 10°C and not more than 120°C.

17. Pertaining to claim 68, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single layer structure or all the two or more insulation unit layers in the insulating layer are formed of an organic material.

18. Pertaining to claim 69, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single-layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of a polyimide resin.

19. Pertaining to claim 70, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of an inorganic material.

20. Pertaining to claim 71, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of a composite composed of an organic material and an inorganic material.

21. Pertaining to claim 72, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single layer structure or all the two or more insulation unit layers in the insulating layer are formed of a polyimide resin.

22. Pertaining to claim 73, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of a low-expansion polyimide having a coefficient of linear thermal expansion of not more than 30 ppm.

23. Pertaining to claim 74, Takashi teaches the process for producing an electronic component according to claim 73, wherein the insulating layer has a layer construction of adhesive polyimide low-expansion polyimide - adhesive polyimide.

24. Pertaining to claim 75, Takashi teaches the process for producing an electronic component according to claim 74, wherein, in the insulating layer having a layer construction of adhesive polyimide - low-expansion polyimide - adhesive polyimide, the two adhesive polyimides are different from each other in composition.

25. Pertaining to claim 76, Takashi teaches the process for producing an electronic component according to claim 57, wherein the etching liquid used for etching the insulating layer has a pH value of more than 9 (i.e. potassium hydroxide is very basic).

26. Pertaining to claim 77, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of copper or surface treated copper.

27. Pertaining to claim 78, Takashi teaches the process for producing an electronic component according to claim 57, wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of copper alloy or surface treated copper alloy.

28. Pertaining to claim 80, Takashi teaches the process for producing an electronic component according to claim 57, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper alloy or surface treated copper alloy.

29. Pertaining to claim 82, Takashi teaches an electronic component produced by the process for producing an electronic component according to any one of claims 57 to 81.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 79, 81 and 83-104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al., Patent Abstracts of Japan Publication number: 2000-183523 in view of Shum et al. U.S. Patent 6,596,184 B1.

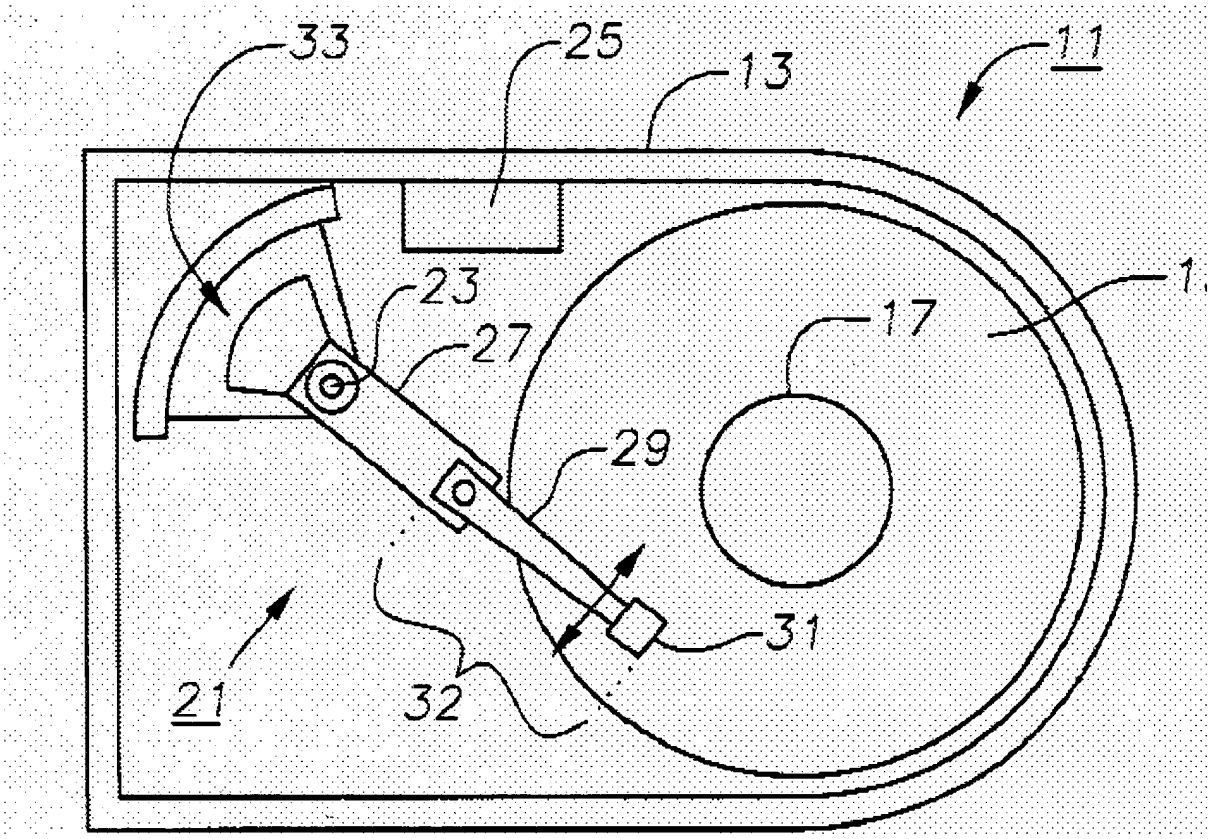
32. Takashi discloses a semiconductor process substantially as claimed.

Pertaining to claim 79, Takashi fails to disclose the process for producing an electronic component according to claim 57, wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of stainless steel or surface treated stainless steel. Shum teaches wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of stainless steel or surface treated stainless steel. See **FIGS. 1-25** where Shum discloses two conductive inorganic materials. In view of Shum, it would have been obvious to one of ordinary skill in the art to incorporate the limitations of Shum into the Takashi semiconductor process because an integrated lead suspension is formed from a laminate of three materials (see Abstract).

33. Pertaining to claim 81, Takashi fails to teach the process for producing an electronic component according to claim 57, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed

of copper or surface treated copper. Shum discloses one of the two conductive inorganic material layers in the laminate is formed of stainless steel and the other is formed of copper. In view of Shum, it would have been obvious to one of ordinary skill in the art to incorporate the limitations of Shum into the Takashi semiconductor process because an integrated lead suspension is formed from a laminate of three materials (see Abstract).

34. Pertaining claim 83, Takashi fails to teach a suspension for a hard disk drive, produced by the process for producing an electronic component according to any one of claims 57 to 81. Shum teaches a suspension for a hard disk drive. . In view of Shum, it would have been obvious to one of ordinary skill in the art to incorporate the limitations of Shum into the Takashi semiconductor process because an integrated lead suspension is formed from a laminate of three materials (see Abstract).



35. Pertaining to claim 84, Takashi fails to disclose a process for producing an electronic component, comprising the steps of:

laminating a laminate of conductive inorganic material layer insulating layer conductive inorganic material layer or a laminate of conductive inorganic material layer - insulating layer onto a dry film; and performing wet etching to produce an electronic component, wherein

the insulating layer in the laminate can be patterned by wet etching,

the insulating layer has a single or multilayer structure,

the thickness of the dry film applied is not less than 1.1 times that of one conductive inorganic material layer in the laminate, and

when the material to be etched is dipped in an

etching liquid held at 70°C, the holding time of the dry film resist pattern is not less than one min. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

36. Pertaining to claim 85, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein at least one side of the dry film resist has fine concaves and convexes.

37. Pertaining to claim 86, Takashi in view of Shum disclose the process for producing an electronic component according to claim 85, wherein the fine concaves and convexes are formed by embossing..

38. Pertaining to claim 87, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the dry film resist is developable with an aqueous alkali solution and can be separated by the aqueous alkali solution.

39. Pertaining to claim 88, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the insulating layer in the laminate is wet etched at a temperature of 10 to 120°C.

40. Pertaining to claim 89, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the etching liquid used for wet etching the insulating layer in the laminate has a pH value of more than 8.

41. Pertaining to claim 90, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the lamination of the dry film onto the laminate followed by wet etching is carried out by a method wherein, after the laminate of the dry film is exposed and developed to perform patterning, in order to improve the resistance of the dry film resist to the etchant for the insulating layer, treatment selected from ultraviolet light irradiation, heat treatment, and a combination of ultraviolet light irradiation with heat treatment is carried out.

42. Pertaining to claim 91, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the whole of one or more layers constituting the insulating layer in the laminate is formed of an organic material.

43. Pertaining to claim 92, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein at least one layer constituting the insulating

layer in the laminate is formed of a composite composed of an organic material and an inorganic material.

44. Pertaining to claim 93, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein at least one layer constituting the insulating layer in the laminate is formed of a polyimide resin.

45. Pertaining to claim 94, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the whole of one or more layers constituting the insulating layer in the laminate is formed of a polyimide resin.

46. Pertaining to claim 95, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein at least one layer constituting the insulating layer in the laminate is a low-expansion polyimide having a coefficient of linear expansion of not more than 30 ppm.

47. Pertaining to claim 96, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the insulating layer in the laminate has a layer construction of adhesive polyimide - low-expansion polyimide - adhesive polyimide.

48. Pertaining to claim 97, Takashi in view of Shum disclose the process for producing an electronic component according to claim 94, wherein, in the insulating layer having a layer

construction of adhesive polyimide - low-expansion polyimide - adhesive polyimide, the two adhesive polyimides are different from each other in composition.

49. Pertaining to claim 98, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the whole of one or two conductive inorganic material layers in the laminate is formed of copper or surface treated copper.

50. Pertaining to claim 99, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the whole of one or two conductive inorganic material layers in the laminate is formed of copper alloy or surface treated copper alloy.

51. Pertaining to claim 100, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein the whole of one or two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel.

52. Pertaining to claim 101, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper alloy or surface treated copper alloy.

53. Pertaining to claim 102, Takashi in view of Shum disclose the process for producing an electronic component according to claim 84, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper or surface treated copper.

54. Pertaining to claim 103, Takashi in view of Shum disclose an electronic component produced by the process for producing an electronic component according to any one of claims 84 to 102.

55. Pertaining to claim 104, Takashi in view of Shum disclose a suspension for a hard disk drive, produced by the process for producing an electronic component according to any one of claims 84 to 102.

Double Patenting

56. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

57. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

58. Claim 57 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 1 of U.S. Patent 6,709,988 B2. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper

after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Conclusion

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

60. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

61. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC